

What is claimed is:

1 1. A memory device with vertical transistors and
2 trench capacitors, comprising:

3 a substrate, having at least one deep trench
4 therein;

5 a trench capacitor, deposited in a lower position of
6 the deep trench;

7 a conducting structure, deposited on the trench
8 capacitor, comprising a first conductive layer
9 and a second conductive layer;

10 a ring shaped insulator, deposited on parts of the
11 sidewall of the deep trench and between the
12 substrate of the deep trench and the first
13 conductive layer, such that the first
14 conductive is surrounded by the ring shaped
15 insulator, wherein the second conductive layer
16 is deposited on the first conductive and the
17 ring shaped insulator;

18 a diffusion barrier, deposited on one side of the
19 sidewall of the deep trench and between the
20 second conductive layer and the substrate of
21 the deep trench;

22 a trench top isolation, deposited on the conducting
23 structure; and

24 a control gate, deposited on the trench top
25 isolation.

1 2. The memory device as claimed in claim 1,
2 further comprising:

3 a buried strap, deposited within the substrate
4 beside parts of the conducting structure where
5 the diffusion barrier is not deposited, serving
6 as a source.

1 3. The memory device as claimed in claim 1,
2 further comprising:

3 a doping area, provided within the substrate beside
4 the control gate, serving as a drain.

1 4. The memory device as claimed in claim 1,
2 wherein the ring shaped insulator comprises an oxide.

1 5. The memory device as claimed in claim 1,
2 wherein the first conductive layer comprises a doped
3 polysilicon or a doped amorphous silicon.

1 6. The memory device as claimed in claim 1,
2 wherein the second conductive layer comprises a doped
3 polysilicon or a doped amorphous silicon.

1 7. The memory device as claimed in claim 1,
2 wherein the diffusion barrier comprises an oxide.

1 8. The memory device as claimed in claim 1,
2 wherein the thickness of the diffusion barrier is
3 substantially less than 100Å.

1 9. The memory device as claimed in claim 1,
2 wherein the trench top isolation comprises an oxide.

1 10. The memory device as claimed in claim 1,
2 wherein the control gate comprises a gate layer and a

3 gate dielectric layer deposited between the gate layer
4 and the substrate.

1 11. The memory device as claimed in claim 1,
2 wherein the gate layer comprises a polysilicon, a
3 silicide, a metal layer, or a combination thereof.

1 12. The memory device as claimed in claim 1,
2 wherein the gate dielectric layer comprises an oxide.

1 13. The memory device as claimed in claim 2,
2 wherein the buried strap is electrically connected with
3 the control gate and formed by diffusing dopants of the
4 first conductive layer into the substrate of the trench
5 surrounding the top of the second conductive layer.

1 14. A method of fabricating a memory device with
2 vertical transistors and trench capacitors, comprising:
3 providing a substrate;
4 forming at least one deep trench in the substrate;
5 forming a trench capacitor in a lower position of
6 the deep trench;
7 forming a ring shaped insulator on the sidewall of
8 the deep trench above the trench capacitor,
9 wherein a space is surrounded by the ring
10 shaped insulator ;
11 forming a first conductive layer to fill the space;
12 forming a diffusion barrier on one side of the
13 sidewall of the deep trench above the ring
14 shaped insulator;

15 forming a second conductive layer on the first
16 conductive layer and the ring shaped insulator
17 and beside the diffusion barrier;
18 forming a trench top isolation on the second
19 conductive layer and the diffusion barrier; and
20 forming a control gate on the trench top isolation.

1 15. The method as claimed in claim 14, further
2 comprising:

3 forming a buried strap within the substrate beside
4 parts of the second conductive layer where the
5 diffusion barrier is not deposited to serve as
6 a source.

1 16. The method as claimed in claim 14, further
2 comprising:

3 forming a doping area within the substrate beside
4 the control gate to serve as a drain.

1 17. The method as claimed in claim 14, wherein the
2 ring shaped insulator comprises an oxide.

1 18. The method as claimed in claim 14, wherein the
2 first conductive layer comprises a doped polysilicon or a
3 doped amorphous silicon.

1 19. The method as claimed in claim 14, wherein the
2 second conductive layer comprises a doped polysilicon or
3 doped amorphous silicon.

1 20. The method as claimed in claim 14, wherein the
2 diffusion barrier comprises an oxide.

1 21. The method as claimed in claim 14, wherein the
2 thickness of the diffusion barrier is substantially less
3 than 100Å.

1 22. The memory device as claimed in claim 14,
2 wherein the trench top isolation comprises an oxide.

1 23. The method as claimed in claim 14, wherein the
2 control gate comprises a gate layer and a gate dielectric
3 layer deposited between the gate layer and the substrate.

1 24. The method as claimed in claim 14, wherein the
2 gate layer comprises a polysilicon, a silicide, a metal
3 layer, or a combination thereof.

1 25. The method as claimed in claim 13, wherein the
2 gate dielectric layer comprises an oxide.

1 26. The method as claimed in claim 15, wherein the
2 buried strap is formed by diffusing the dopants of the
3 first conductive layer into the substrate during
4 annealing so as to electrically connect with the control
5 gate.

1 27. A method of fabricating a memory device with
2 vertical transistors and trench capacitors, comprising:
3 providing a substrate;
4 forming at least one deep trench in the substrate;
5 forming a trench capacitor in a lower position of
6 the deep trench;
7 forming a ring shaped insulator on the sidewall of
8 the deep trench above the trench capacitor,

9 wherein a space is surrounded by the ring
10 shaped insulator ;
11 forming a first conductive layer to fill the space;
12 performing a nitridation in the substrate of the
13 bottom and one side of the sidewall of the deep
14 trench;
15 performing a oxidation in the substrate of the
16 bottom and the sidewall of the deep trench to
17 form a thick oxide layer and a thin oxide
18 layer, wherein the thin oxide layer is formed
19 on parts of the substrate where nitridation has
20 been performed, the thick oxide layer is formed
21 on parts of the substrate without nitridation;
22 removing the thin oxide layer;
23 forming a second conductive layer on the first
24 conductive layer and the ring shaped insulator;
25 etching parts of the thick oxide layer using the
26 second conductive layer as a mask so as to form
27 a diffusion barrier between the second
28 conductive layer and one side of the sidewall
29 of the trench;
30 forming a trench top isolation on the second
31 conductive layer and the diffusion barrier; and
32 forming a control gate on the trench top isolation.

1 28. The method as claimed in claim 27, further
2 comprising:

3 forming a buried strap within the substrate beside
4 parts of the second conductive layer where the

5 diffusion barrier is not deposited to serve as
6 a source.

1 29. The method as claimed in claim 27, further
2 comprising:

3 forming a doping area within the substrate beside
4 the control gate to serve as a drain.

1 30. The method as claimed in claim 27, wherein the
2 ring shaped insulator comprises an oxide.

1 31. The method as claimed in claim 27, wherein the
2 first conductive layer comprises a doped polysilicon or
3 doped amorphous silicon.

1 32. The method as claimed in claim 27, wherein the
2 second conductive layer comprises a doped polysilicon or
3 doped amorphous silicon.

1 33. The method as claimed in claim 27, wherein the
2 diffusion barrier comprises an oxide.

1 34. The method as claimed in claim 27, wherein the
2 thickness of the diffusion barrier is substantially less
3 than 100Å.

1 35. The method as claimed in claim 27, wherein the
2 trench top isolation comprises an oxide.

1 36. The method as claimed in claim 27, wherein the
2 control gate comprises a gate layer and a gate dielectric
3 layer deposited between the gate layer and the substrate.

1 37. The method as claimed in claim 27, wherein the
2 gate layer comprises a polysilicon, a silicide, a metal
3 layer, or the combination thereof.

1 38. The method as claimed in claim 36, wherein the
2 gate dielectric layer comprises an oxide.

1 39. The method as claimed in claim 28, wherein the
2 buried strap is formed by diffusing the dopants of the
3 first conductive layer into the substrate during
4 annealing so as to electrically connect with the control
5 gate.

1 40. The method as claimed in claim 27, wherein the
2 nitridation is performed by nitrogen-containing ion
3 implantation into the substrate according a certain
4 tilting angle.

1 41. The method as claimed in claim 40, wherein the
2 certain tilting angle is about 5~10°.

1 42. The method as claimed in claim 27, wherein the
2 oxidation is performed by thermal oxidation.